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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,753	09/13/2000	Chin-Huang Chang	6319-56134	7237

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EXAMINER

VINH, LAN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 07/03/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/66Q,753

Applicant(s)

CHANG, CHIN-HUANG

Examiner

LAN VINH

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 8-11, 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dery et al (US 6,074,895) in view of Hudak et al (US 5,656,552)

Dery discloses a method for forming a semiconductor flip-chip assembly/package having chip carrier 220, the semiconductor flip-chip assembly includes IC chip/semiconductor unit having a first surface 211 and second surface 210 above the first surface (fig. 2B). This method comprises the step of:

joining/attaching the first surface 211 of a IC chip/semiconductor unit to a chip carrier/seating apparatus 220 , the first surface 211 faces chip carrier 220 whereas the second surface 210 of the IC chip is exposed. The IC chip is joined to the chip carrier 220 via contact pads/leads 226 on the chip carrier(leads-on-chip configuration) (col 5, lines 41-47 and fig. 2D)

using RIE (reactive ion etching) plasma to modify the second surface 210 of the IC chip/semiconductor unit (col 5, lines 51-55 and fig. 2C) reads on etching the semiconductor unit from a second surface of the semiconductor unit .

Unlike the instant claimed invention as per claims 1, 11, Dery does not specifically disclose etching the second surface of the IC chip/semiconductor unit until the size (

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thickness) of the semiconductor unit meets an expected specification/a specified range of thickness between 2 mil-6mil. The claimed term "an expected specification" is defined as a thickness ranging from 2 mil-6mil in line 8 on page 7 of the instant specification.

However, Hudak discloses a method for making thin conformal IC chip module comprises the step of using RIE etching/plasma etching to thin down the thickness of the IC chip to 50 microns or approximately 2 mil (25.4 microns equal 1 mil) (see prior art of record for evidence of this basis) (col 8, lines 20-22). Husak's etching step reads on etching the surface of the IC chip/semiconductor unit until the size (thickness) of the semiconductor unit meets an expected specification/a specified range of thickness between 2 mil-6mil.

Since both Dery and Hudak are concerned with method using RIE etching to modify/reduce the thickness of a IC chip, one skilled in the art at the time the invention was made would have found it obvious to modify Dery by using the step of etching the surface of the IC chip/semiconductor unit until the size (thickness) of the semiconductor unit meets an expected specification/a specified range as per Hudak especially since Hudak discloses that by thinning the IC chip/die to a thickness less than or equal to 50 microns/ 2mil , a planarization step required by prior art method may be eliminated (col 4, lines 65-67)

Regarding claims 2, 3,12, Dery discloses plasma RIE etching using oxygen gas (col 3, lines 59-61)

The limitation as recited in claim 4 has been discussed above in paragraph 2.

Regarding claim 5, Dery discloses joining/attaching the chip to the carrier using solder bump/bump connection (col 4, lines 19-21)

Regarding claims 6, 8, Dery discloses using the laminate 122/ fixture to cover/shield the chip carrier 120 before etching (col 4, lines 11-12)

Regarding claim 9, in one embodiment Dery discloses joining/attaching the IC chip to the chip carrier by contact pads/leads 212 on the IC chip (col 5, lines 44-46) reads on attaching the semiconductor unit/chip to a carrier according to a configuration of lead-on-chip packaging.

Regarding claims 10, 14 Dery discloses using a chip carrier (col 3, line 43), establishing electrical contact between the solder bumps on the first surface 211 to chip carrier 220 (col 5, lines 41-46)

Regarding claims 15, 16, Dery discloses that using epoxy resin/adhesive material between the chip and the chip carrier and the chip is electrically connected to the chip carrier via contact pads/electrical connection device (col 5, lines 44-46)

Regarding claim 17, Dery discloses using the laminate 122 to cover/shield the chip carrier 120 before etching (col 4, lines 11-12) reads on shielding the chip carrier from etching.

Regarding claim 18, Dery discloses electrically connecting the semiconductor unit to the chip carrier after plasma etching step (col 4, lines 64-66)

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3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dery et al (US 6,074,895) in view of Hudak et al (US 5,656,552) and further in view of Shimizu et al (US 6,355,569)

Dery as modified by Hudak has been described above. Dery and Hudak differs from the instant claimed invention as per claim 12 by etching the second surface using plasma etching/dry etching instead of etching using beams of light.

However, Shimizu discloses a dry etching method comprises the step of dry etching/plasma etching using beam of light (see abstract)

Hence, one skilled in the art would have found it obvious to substitute Dery and Hudak method by etching the second surface using beams of light on view of Shimizu's teaching because both plasma etching and etching using beam of light are known dry etching method , thus the substitution of one for the other would have been anticipated to produce an expected result.

4. Claims 7, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dery et al (US 6,074,895) in view of Hudak et al (US 5,656,552) and further in view of Siniaguine (US 6,184,060)

Dery as modified by Hudak has been described above in paragraph 2. Unlike the instant claimed inventions as per claims 7, 13, Dery and Hudak do not disclose the step of grinding the IC chip/semiconductor unit to a expected specification/ a specified thickness range before joining the IC chip to the carrier.

However, Siniaguine discloses a method for fabricating semiconductor die comprises the step of grinding the semiconductor wafer to reduce the thickness to a specified thickness before dicing the wafer into chip (col 8, lines 48-50)¹

Hence, one skilled in the art would have found it obvious to modify Dery and Hudak by adding the step of grinding the semiconductor wafer to reduce the thickness as per Siniaguine since Siniaguine states that silicon is removed from the semiconductor wafer/semiconductor unit by known method such as mechanical grinding to reduce the wafer thickness to a specified range (col 8, lines 47-50)

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (US 6,184,060) in view of Shimizu et al (US 6,355,569)

Siniaguine discloses a method for fabricating semiconductor chip/die, the die having a first surface and second surface. This method comprises the steps of:

dicing the wafer into a plurality of chips/die (col 8, lines 50-51)

placing/moving the chip/die into the chip holder/seating apparatus to expose one surface of the die (col 8, lines 56-58)

plasma etching the chip/die to thin/reduce the thickness of the exposed surface of the chip/die (col 8, lines 52-54), fig. 18 shows that the chip holder 1610/seating apparatus shielding one surface of the chip/die from being etched /immunizing one surface of the chip/die against etching

Siniaguine differs from the instant claimed invention as per claim 19 by etching the die using plasma etching/dry etching instead of etching using beams of light.

However, Shimizu discloses a dry etching method comprises the step of dry etching/plasma etching using beam of light (see abstract)

Hence, one skilled in the art would have found it obvious to modify Siniaguine method by etching the die using beams of light on view of Shimizu's teaching because both plasma etching and etching using beam of light are known dry etching method , thus the substitution of one for the other would have been anticipated to produce an expected result.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (US 6,184,060) in view of Shimizu et al (US 6,355,569) and further in view of Hudak et al (US 5,656,552)

Siniaguine as modified by Shimizu has been described above. Unlike the instant claimed invention as per claim 20, Siniaguine and Shimizu do not specifically discloses stopping the etching step when the size (thickness) of chip/die meets an expected specification/a specified range of thickness between 2 mil-6mil. The claimed "an expected specification" is defined as a thickness ranging from 2 mil-6mil in line 8 on page 7 of the instant specification.

However, Hudak discloses a method for making thin conformal IC chip module comprises the step of using RIE etching/plasma etching to thin down the thickness of the IC chip/die to 50 microns or approximately 2 mil (25.4 microns equal 1 mil) (see prior art of record for evidence of this basis) (col 8, lines 20-22). Husak's etching step

reads on stopping the etching when the size (thickness) of the IC chip meets an expected specification/a specified range of thickness between 2 mil-6mil.

Since both Siniaguine and Hudak are concerned with method using plasma etching to reduce the thickness of a IC chip, one skilled in the art at the time the invention was made would have found it obvious to modify Siniaguine and Shimizu by stopping the etching when the size (thickness) of the semiconductor unit meets an expected specification/a specified range as per Hudak especially since Hudak discloses that by thinning the IC chip/die to a thickness less than or equal to 50 microns/ 2mil , a planarization step required by prior art method may be eliminated (col 4, lines 65-67)

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Myer et al (US 4,872,945) discloses that 25.4 microns being equal to 1mil (col 5, lines 20-22)

Response to Arguments

8. Applicant's arguments filed 6/3/2002 have been fully considered but they are not persuasive.

In traversing the examiner rejection of claim 1, the applicants argue that Dery does not disclose any suggestion of reducing the size of the semiconductor unit by plasma etching. The examiner disagrees because although Dery does not explicitly discloses reducing the size of the semiconductor unit by plasma etching, Dery clearly discloses

using the plasma etching to modify the surface of the semiconductor unit (col 3, lines 64-65). Since etching is known in the art as a process of removing material/ reducing thickness of a material layer from the substrate, Dery's teaching of plasma etching to modify the surface of the semiconductor unit, as interpreted by the examiner, reads on reducing the size/thickness of the semiconductor unit by plasma etching.

It is also argued that Dery does not disclose using the chip carrier as a seating apparatus when etching the semiconductor unit because in Fig. 2C of Dery, the electrodes 232 instead of chip carrier 220 acts as a seating apparatus for the chip 210 to be treated by plasma. This argument is not found persuasive because as clearly shown in fig. 2C of Dery, the semiconductor device 210 is seated on the chip carrier layer 220 and the chip carrier 220 is placed on the electrodes 232 in the plasma chamber. Based on what is disclosed in Fig. 2C of Dery, the examiner asserts that the chip carrier acts as a seating apparatus for chip 210 during plasma treatment.

9. Applicant's amendment necessitated the new ground(s) of rejection of claims 12, 19, 20 presented in this Office action. The examiner maintained the same ground of rejection regarding independent claims 1, 11. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAN VINH whose telephone number is 703 305-6302. The examiner can normally be reached on Monday-Friday 8:30 -6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BENJAMIN L UTECH can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
June 30, 2002


BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700